WHAT IS CLAIMED IS:

1. A flag combining circuit, comprising:

an analysis circuit that receives a plurality of operands each of which having encoded status flag information, the analysis circuit being operative to analyze the plurality of operands and to provide an indication of one or more predetermined formats in which the plurality of operands are represented; and

a result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands.

2. The flag combining circuit of claim 1, wherein at least one of the plurality of operands is a floating point operand.

3. The flag combining circuit of claim 1, further comprising one or more operand buffers that receive the plurality of operands and transfers them to the analysis circuit.

4. The flag combining circuit of claim 1, further comprising a decision circuit that receives the indication from the analysis circuit and provides a second indication to the result assembler.

5. The flag combining circuit of claim 1, wherein the predetermined formats represent a zero format, an overflow format, an underflow format, a denormalized format, a normalized non-zero format, an infinity format, and a not-a-number (NaN) format.

6. The flag combining circuit of claim 1, wherein encoded status flag information represents an invalid operation flag, an overflow flag, an underflow flag, a division by zero flag, and an inexact flag.

7. The flag combining circuit of claim 5, wherein the overflow format represents one of a +OV status and a -OV status.

8. The flag combining circuit of claim 7, wherein the overflow format includes a set inexact status flag.

9. The flag combining circuit of claim 5, wherein the underflow format represents one of a +UN status and a -UN status.

10. The flag combining circuit of claim 9, wherein the underflow format includes a set inexact status flag.

11. The flag combining circuit of claim 5, wherein a least significant bit in the plurality of operands represents a set inexact status flag.

12. The flag combining circuit of claim 1, wherein the accumulated result produced is assembled using one of a commutative and an associative flag-combining operation.

13. The flag combining circuit of claim 1, wherein the accumulated result produced is in a NaN format.

14. The flag combining circuit of claim 13, wherein at least one of the plurality of operands is in the NaN format.

15. The flag combining circuit of claim 1, wherein the accumulated result represents information from one of the plurality of operands that has a larger fraction field.

16. The flag combining circuit of claim 1, wherein a sign bit in the accumulated result is a logical OR of sign bits in the plurality of operands.

17. The flag combining circuit of claim 1, wherein the result assembler produces the accumulated result in a NaN formatted one of the plurality of operands.

18. A method for combining flag information, comprising the steps of:

receiving a plurality of operands, each of which having encoded status flag information;

analyzing the plurality of operands to provide indications of one or more predetermined formats in which the plurality of operands are represented;

generating control signals based on the indications of the one or more predetermined formats; and

assembling an accumulated result based at least upon the generated control signals and input signals, the accumulated result representing a value and combining the encoded status flag information from each of the plurality of operands.

19. The method of claim 18, wherein receiving the plurality of operands includes receiving at least one floating point operand.

20. The method of claim 18, wherein analyzing the plurality of operands includes providing an indication of predetermined formats representing a zero format, an overflow format, an underflow format, a denormalized format, a normalized non-zero format, an infinity format, and a not-a-number (NaN) format.

21. The method of claim 18, wherein encoded status flag information represents an invalid operation flag, an overflow flag, an underflow flag, a division by zero flag, and an inexact flag.

22. The method of claim 20, wherein the overflow format represents one of a +OV status and a -OV status.

23. The method of claim 22, wherein the overflow format includes a set inexact status flag.

24. The method of claim 20, wherein the underflow format represents one of a +UN status and a -UN status.

25. The method of claim 24, wherein the underflow format includes a set inexact status flag.

26. The method of claim 18, wherein assembling the accumulated result includes using one of a commutative and an associative flag-combining operation.

27. The method of claim 18, wherein assembling the accumulated result produces a result in a not-a-number (NaN) format.

28. The method of claim 27, wherein at least one of the plurality of operands is in the NaN format.

29. The method of claim 18, wherein assembling the accumulated result includes using at least two of the plurality of operands in a NaN format.

30. The method of claim 29, wherein assembling the accumulated result includes representing information from which of the at least two of the plurality of operands has a larger fraction field.

31. The method of claim 18, wherein a sign bit in the accumulated result is a logical OR of sign bits in the plurality of operands.

32. The method of claim 18, wherein assembling the accumulated result includes producing the accumulated result in a NaN formatted one of the plurality of operands.

33. A computer-readable medium on which is stored a set of instructions for combining operands, which when executed perform steps comprising:

receiving a plurality of operands, each of which having encoded status flag information;

analyzing the plurality of operands to provide indications of one or more predetermined formats in which the plurality of operands are represented;

generating control signals based on the indications of the one or more predetermined formats; and

assembling an accumulated result based at least upon the generated control signals and input signals, the accumulated result representing a value and combining the encoded status flag information from each of the plurality of operands.

34. The computer-readable medium of claim 33, wherein receiving the plurality of operands includes receiving at least one floating point operand.

35. The computer-readable medium of claim 33, wherein analyzing the plurality of operands includes providing an indication of predetermined formats representing a zero format, an overflow format, an underflow format, a denormalized format, a normalized non-zero format, an infinity format, and a not-a-number (NaN) format.

36. The computer-readable medium of claim 33, wherein encoded status flag information represents an invalid operation flag, an overflow flag, an underflow flag, a division by zero flag, and an inexact flag.

37. The computer-readable medium of claim 35, wherein the overflow format represents one of a +OV status and a -OV status.

38. The computer-readable medium of claim 37, wherein the overflow format includes a set inexact status flag.

39. The computer-readable medium of claim 35, wherein the underflow format represents one of a +UN status and a -UN status.

40. The computer-readable medium of claim 39, wherein the underflow format includes a set inexact status flag.

41. The computer-readable medium of claim 33, wherein assembling the accumulated result includes using one of a commutative and an associative flag-combining operation.

42. The computer-readable medium of claim 33, wherein assembling the accumulated result produces a result in a not-a-number (NaN) format.

43. The computer-readable medium of claim 42, wherein at least one of the plurality of operands is in the NaN format.

44. The computer-readable medium of claim 33, wherein assembling the accumulated result includes using at least two of the plurality of operands in a NaN format.

45. The computer-readable medium of claim 44, wherein assembling the accumulated result includes representing information from which of the at least two of the plurality of operands has a larger fraction field.

46. The computer-readable medium of claim 33, wherein a sign bit in the accumulated result is a logical OR of sign bits in the plurality of operands.

47. The computer-readable medium of claim 33, wherein assembling the accumulated result includes producing the accumulated result in a NaN formatted one of the plurality of operands.